# On the Enlargement of Single Event Transients' Width in Flash-based FPGAs

***Authors:*** N. Battezzati, L. Sterpone, M. Violante (*Politecnico di Torino*),
S. Gerardin, A. Manuzzato, A. Paccagnella (*Università di Padova*),
S. Rezgui (*Actel Corp.*), D. Merodio, R. Sorensen, C. Poivey (*ESA*)

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# Outline

- The goals of this work
- Background
- The proposed methodology
- A case study
- Experimental results
- Conclusions and future works

# The goals of the work

- Analysis of the robustness of designs implemented in Flash-based FPGAs
- Study of transient faults effects in safety- and mission-critical designs

# Flash-based FPGAs

- FPGAs capable of in-the-field modifications to the configuration of:
  - Programmable logic blocks (VersaTiles)
  - Programmable interconnections
- The configuration memory is manufactured using the Flash memory technology.

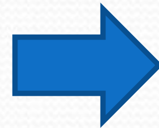
# Radiation effects in Flash-based FPGAs

- Configuration memory of Flash-based FPGAs cannot be upset, because of the technology and the cell size

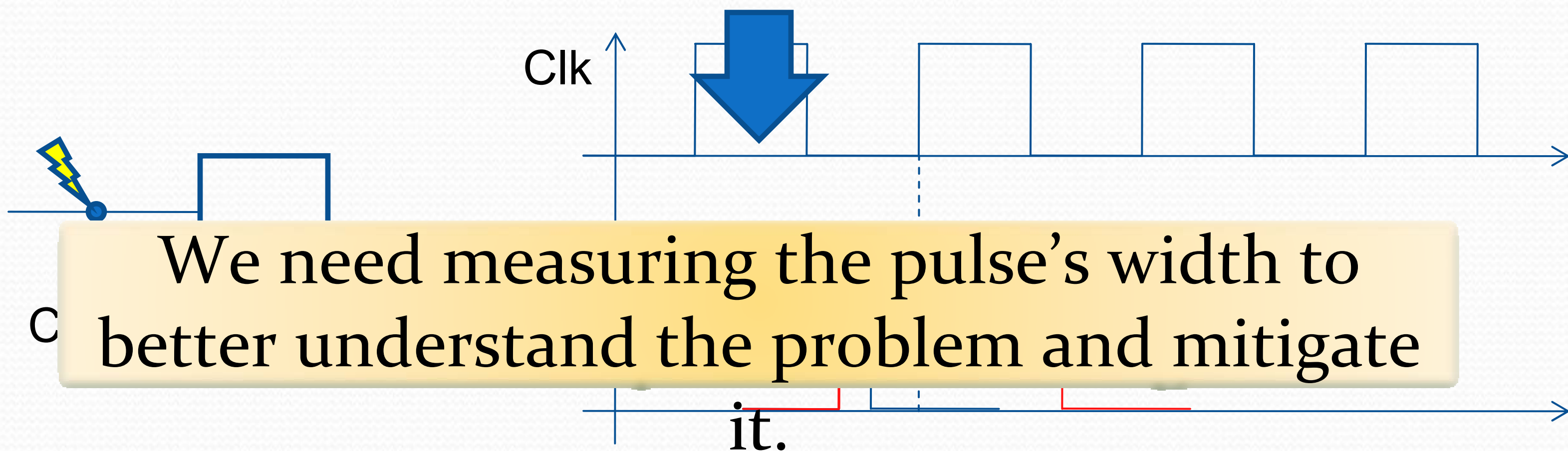
- Single Event Transients (SETs) become more relevant.

# Transient effects

- The effect of an SET is mainly due to:
  - Location
  - Arrival time
  - Pulse's width.



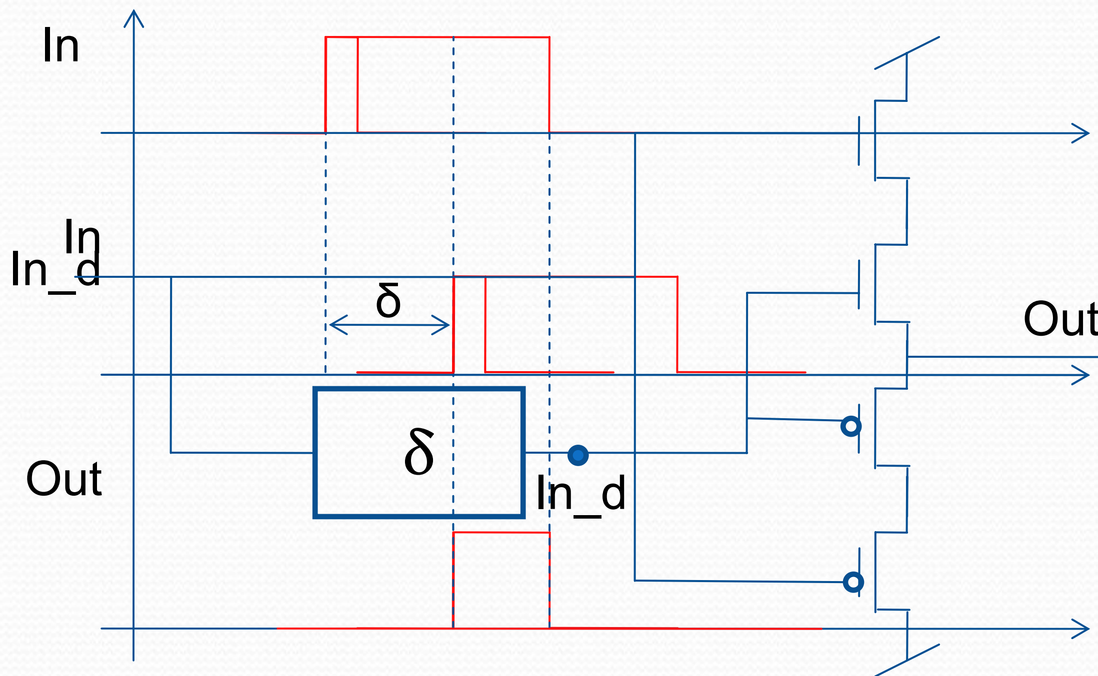
Infinite number of combinations



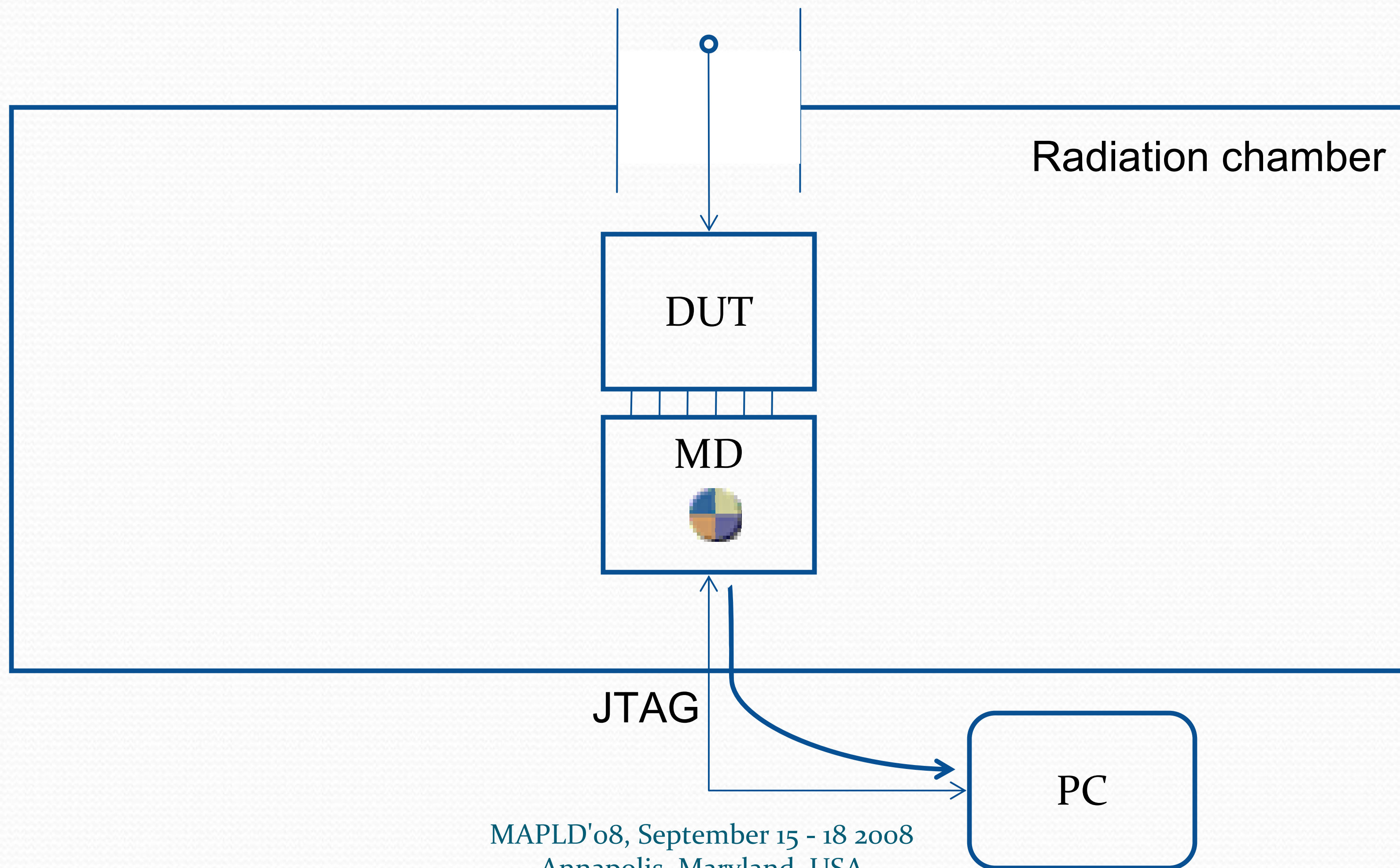

We need measuring the pulse's width to better understand the problem and mitigate it.

# Background

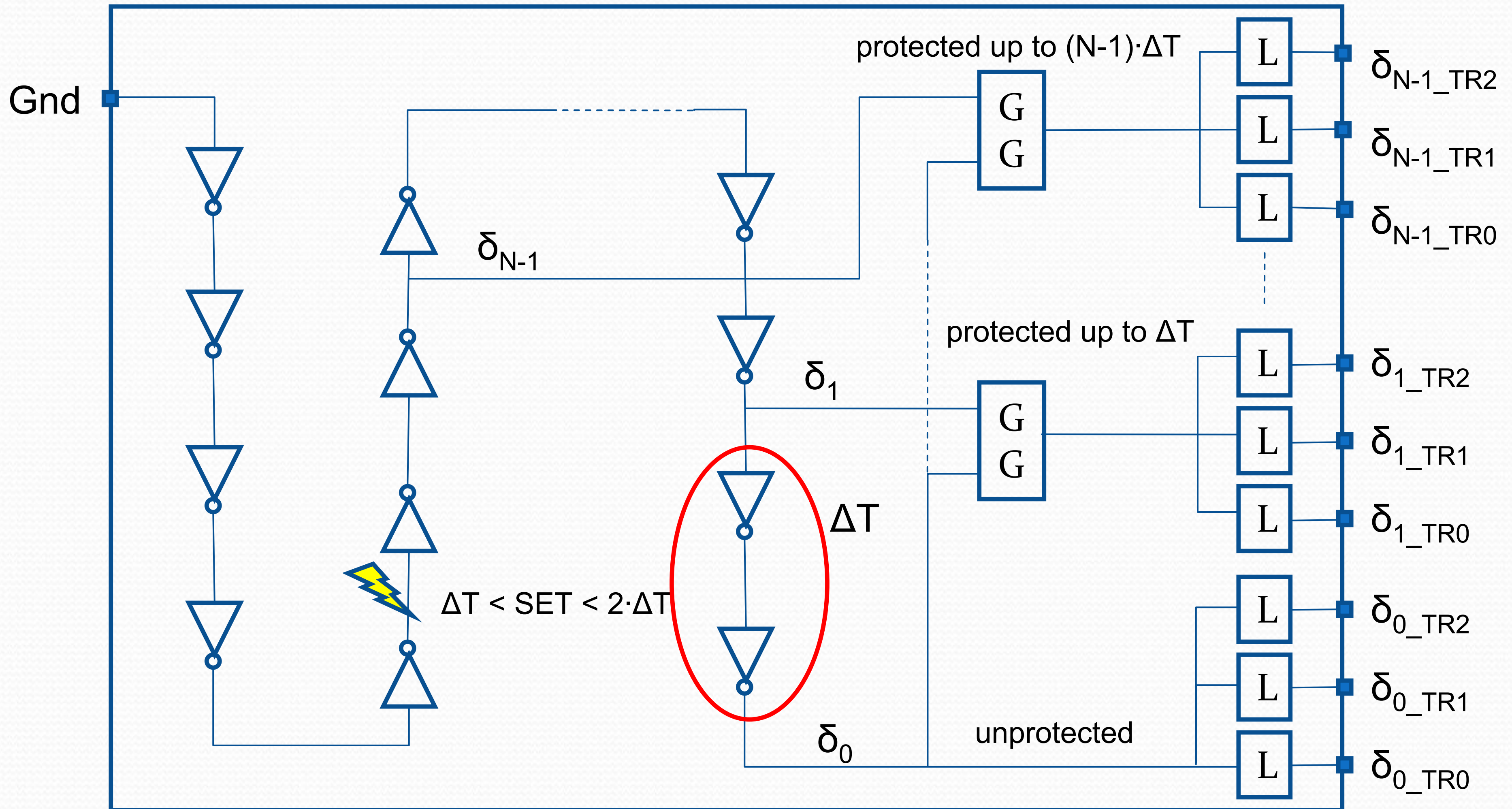
- Guard gate mitigation technique



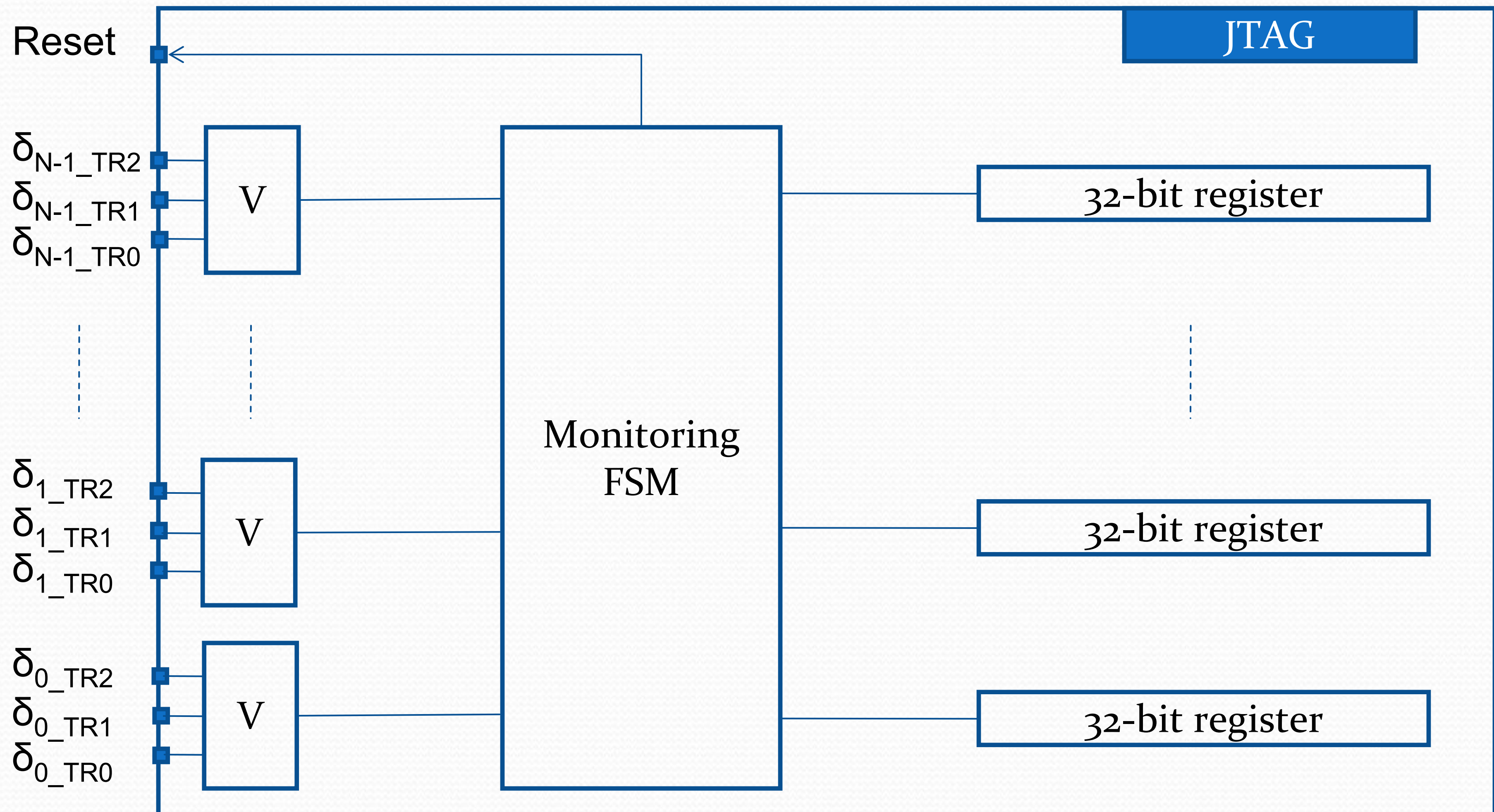
# The proposed methodology



# The DUT Design



# The Monitoring Design



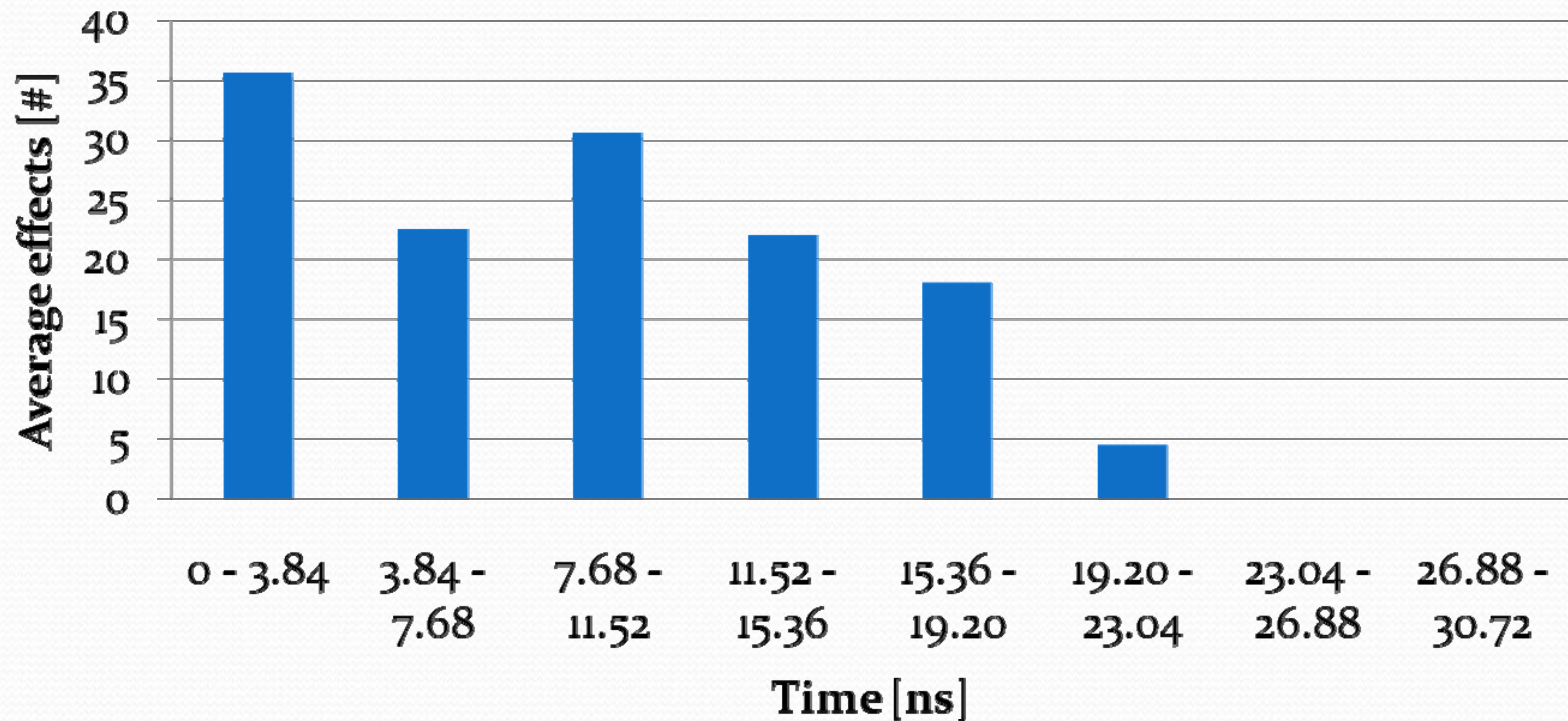
# Design challenges

- Different I/O banks
- Blind time
- Design cross-section
- Number of voted channels, $\delta_0 \ldots \delta_{N-1}$

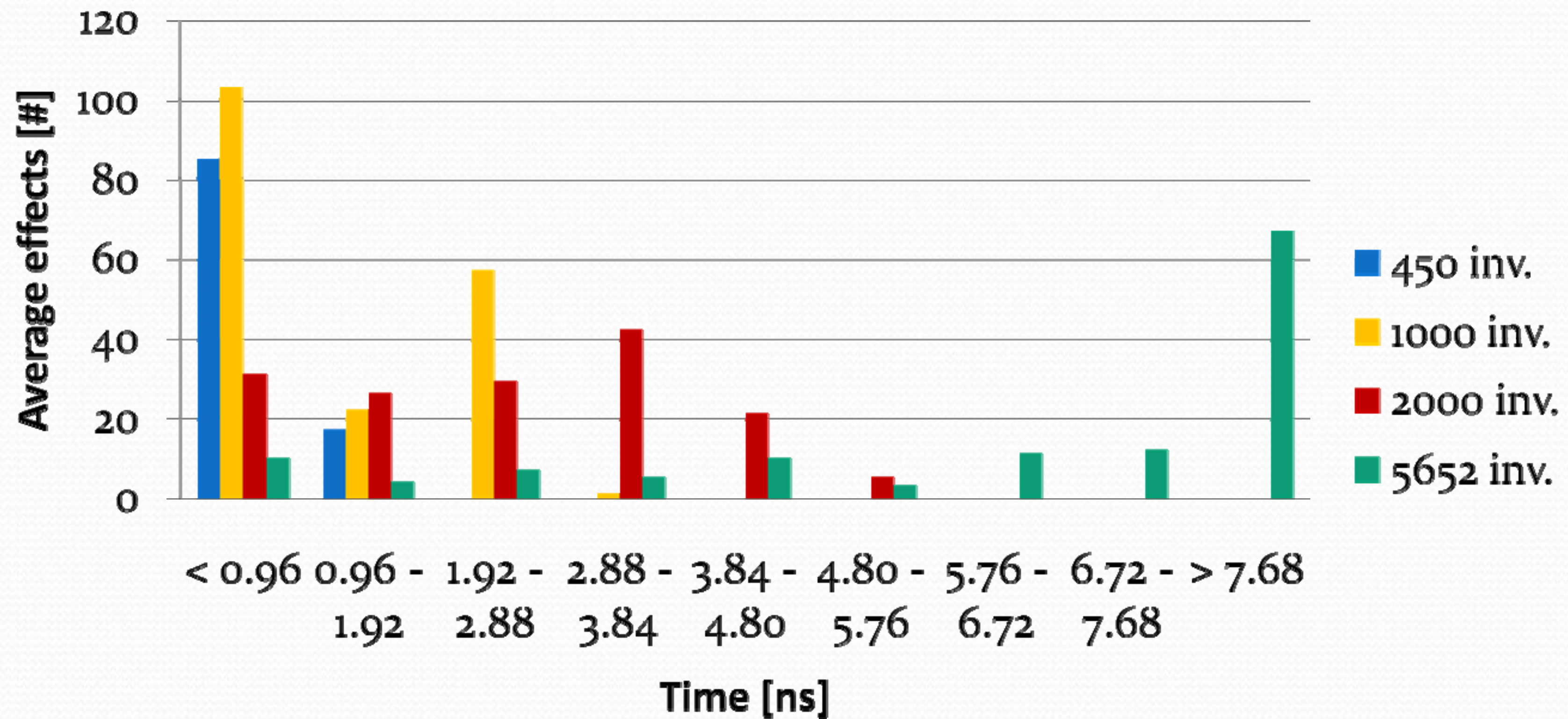
# A case study

- DUT: Actel ProASIC3 250
  - 6,144 VersaTiles
  - A single chain composed of 5,652 inverters (> 90% VersaTiles)
  - 9 channels, $\Delta T = 0.96$ ns
- MD: Xilinx Virtex-II Pro 4
  - 100 MHz clock → blind time ≈ 20 ns
  - Partial readback capability
  - Full support for 1149.1 IEEE standard (Boundary Scan)
- Ion beams: Louvain-la-Neuve, Belgium
  - Xe ions, LET = 55.9 MeV·cm$^2$/mg, different fluences

# Experimental results



# Experimental results



# Conclusions

- We developed a method for evaluating SETs' effects width
  - Independently from the Device Under Test
  - With a very low cost

- The method has been validated comparing it against Actel Corporation's results.

# Future works

- Evaluation of transient effects in *real* designs
  - Investigation of the actual impact of SETs wrt SEUs in real designs
  - Investigation of SETS effects wrt different placement schemes

- Evaluation of hardening techniques effectiveness in real designs

- Development of an *automatic tool* for analyzing and hardening designs implemented in Flash-based FPGAs.

Thank you for your attention